In the Claims

1. (original) An NROM memory transistor comprising:
   a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
   a nanolaminate, high permittivity (high-k), metal gate dielectric formed by an oxidation of metal overlying the substrate, the gate dielectric having a dielectric constant greater than a dielectric constant of silicon dioxide; and
   a control gate formed on top of the gate dielectric.

2. (original) The transistor of claim 1 wherein the gate dielectric is a composite oxide – high-k dielectric – oxide nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer formed by low temperature oxidation of metal.

3. (original) The transistor of claim 1 wherein the gate dielectric is a composite oxide – oxide – high-k dielectric nanolaminate gate insulator wherein the nitride layer is a charge trapping layer formed by low temperature oxidation of metal.

4. (original) The transistor of claim 1 wherein the transistor is used in either a NOR-type flash memory structure or a NAND-type flash memory structure.

5. (original) The transistor of claim 2 wherein the charge trapping layer is comprised of a material that has a lower conduction band edge than silicon nitride.

6. (original) The transistor of claim 2 wherein the gate dielectric has a larger energy barrier between the high-k dielectric and the oxide insulator than silicon dioxide.

7. (original) The transistor of claim 1 wherein the gate dielectric is comprised of one of the following structures: oxide – oxidized Hf – oxide, oxide – oxidized Zr – oxide, or oxide – oxidized Al – oxide.

8. (original) An NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer formed by oxidation of metals overlying the substrate and substantially between the plurality of source/drain regions, the gate insulator comprising a trapping layer having a higher dielectric constant than silicon dioxide; and

a control gate formed on top of the gate insulator layer.

9. (original) The transistor of claim 8 wherein the composite gate insulator comprises an oxide – oxide – high-k dielectric structure.

10. (original) The transistor of claim 8 wherein the composite gate insulator comprises a perovskite oxide film.

11. (original) The transistor of claim 8 wherein the composite gate insulator comprises a stack of oxide films having properties of high dielectric constant (k) oxide – low-k oxide – high-k oxide.

12. (original) The transistor of claim 8 wherein the composite gate insulator is formed by low temperature oxidation.

13. (original) The transistor of claim 8 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.

14. (original) The transistor of claim 8 wherein the control gate is a polysilicon material.

15. (original) The transistor of claim 8 wherein the substrate is comprised of a p+ type silicon material.

16. (original) The transistor of claim 8 wherein the composite gate insulator layer is comprised of one of the following structures: oxide – oxide – Al_2O_3, oxide – oxide – HfO_2, or oxide – oxide – ZrO_2 wherein the metal oxide layers are formed by low temperature oxidation.

17. (original) An NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a nanolaminate, high permittivity, oxidized metal gate insulator layer formed by low temperature oxidation overlying the substrate, the gate insulator comprising a structure having a plurality of layers each having a dielectric constant that is higher than silicon dioxide; and

a control gate formed on top of the gate insulator layer.

18. (original) The transistor of claim 17 wherein the substrate is comprised of a p+ type conductivity silicon and the source/drain regions are n+ doped regions in the substrate and the gate insulator is formed substantially between the source/drain regions.

19. (original) An NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a nanolaminate, high permittivity, oxidized metal gate insulator layer formed by low temperature oxidation overlying the substrate, the gate insulator comprising a structure having a plurality of layers each having a different dielectric constant properties; and

a control gate formed on top of the gate insulator layer.

20. (original) An electronic system comprising:

a processor that generates control signals; and

a memory array coupled to the processor, the array comprising a plurality of NROM memory cells, each NROM memory cell comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;

a nanolaminate, high permittivity (high-k), metal gate dielectric formed by an oxidation of metal overlying the substrate, the gate dielectric having a dielectric constant greater than a dielectric constant of silicon dioxide; and

a control gate formed on top of the gate dielectric.

21. (original) A method for fabricating an NROM memory cell, the method comprising:

creating a plurality of source/drain regions by doping portions of a substrate;

forming a nanolaminate gate insulator on the substrate, the gate insulator having a dielectric constant that is higher than silicon dioxide;

low temperature oxidizing at least one metal layer of the nanolaminate gate insulator; and

forming a control gate on the oxide insulator material.

22. (original) The method of claim 21 wherein the plurality of source/drain regions are created with a p+ conductivity in an n+ substrate.

23. (original) The method of claim 21 wherein the gate insulator is comprised of an oxide – high-k dielectric – oxide structure.

24. (original) The method of claim 21 wherein the gate insulator is comprised of an oxide – oxide – high-k dielectric structure.

25. (original) The method of claim 21 wherein the gate insulator is comprised of a high-k dielectric – high-k dielectric – high-k dielectric structure.

26. (original) The method of claim 21 wherein forming the gate insulator comprises forming one of the following structures: oxide –HfO_2 – oxide, oxide – ZrO_2 – oxide, or oxide – Al_2O_3 – oxide.

27. (original) The method of claim 21 wherein forming the gate insulator comprises forming one of the following structures: oxide – oxide – Al_2O_3, oxide – oxide – HfO_2, or oxide – oxide – ZrO_2

28. (original) The method of claim 21 wherein forming the gate insulator comprises an atomic layer deposition technique prior to the low temperature metal oxidation.

29. (original) The method of claim 21 wherein forming the gate insulator comprises an evaporation technique prior to the low temperature metal oxidation.

30. (original) The method of claim 21 wherein forming the gate insulator comprises an atomic layer deposition technique and an evaporation technique prior to the low temperature metal oxidation.

31. (original) A method for fabricating an NROM memory cell, the method comprising:
creating a plurality of source/drain regions by doping portions of a substrate;
forming a tunnel oxide layer on the substrate;
forming a gate dielectric layer with a low temperature metal oxidation technique on the tunnel oxide layer, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide;
forming an oxide layer on the gate dielectric layer; and
forming a control gate on the oxide insulator material.

32. (original) The method of claim 31 wherein forming the gate dielectric layer further comprises evaporating one of the following materials: HfO_2, ZrO_2, $LaAlO_3$, Y_2O_3, Gd_2O, TiO_2, $CrTiO_3$, or YSiO.

33. (original) A method for fabricating an NROM memory cell, the method comprising:
creating a plurality of source/drain regions by doping portions of a substrate;
forming a tunnel oxide layer on the substrate;
forming a gate dielectric layer using a low temperature metal oxidation on the tunnel oxide layer, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide;
forming an oxide layer on the gate dielectric layer; and
forming a control gate on the oxide insulator material.

34. (original) The method of claim 33 wherein the gate dielectric layer comprises atomic layer deposition of one of the following materials: HfO_2, ZrO_2, Al_2O_3, La_2O_3, $LaAlO_3$, $HfAlO_3$, Ta_2O_5, TiO_2, or Pr_2O_3.

35. (original) A method for fabricating an NROM memory cell, the method comprising:
creating a plurality of source/drain regions by doping portions of a substrate;
forming a tunnel oxide layer on the substrate;
forming a nitride layer on the tunnel oxide layer; and
forming a gate dielectric layer with a low temperature metal oxidation technique on the nitride layer, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide;
forming a control gate on the oxide insulator material.

36. (original) The method of claim 35 wherein forming the gate dielectric layer comprises deposition of one of the following materials: Al_2O_3, HfO_2, or ZrO_2 wherein the metal is oxided by low temperature oxidation.

37. (original) A method for fabricating an NROM memory cell, the method comprising:
creating a plurality of source/drain regions by doping portions of a substrate;

forming a nanolaminate gate dielectric layer with a low temperature metal oxidation technique on the substrate, the gate dielectric layer having a dielectric constant that is higher than silicon dioxide; and

forming a control gate on the oxide insulator material.

48. (currently amended) The method of claim ~~39~~ 37 wherein the gate dielectric layer is formed on the substrate substantially between the source/drain regions.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and Applicant believes no additional fee is required by this Response to Notice of Non-Compliant Amendment.

Respectfully submitted,

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